AF/2815

Attorney's Docket No.: 06618-590001 / CIT- 3165

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: A. E. Bolotnikov et al. Art Unit :2815
Serial No.:09/933,349 Examiner :J. Jackson, Jr.
Filed : February 23, 2001
Title : INDIUM FEATURES ON MULTI-CONTACT CHIPS

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

BRIEF ON APPEAL

Applicant herewith files this brief on appeal within one month of the mailing of the Notice of Panel Decision from Pre-Appeal Brief Review, thereby perfecting the Notice of Appeal that was filed on August 31, 2005. The sections required by the rules follow.

(1) Real Party in Interest

This application is assignee to the California Institute of Technology, a non-profit university in Pasadena, CA.

(2) Related Appeals and Interferences

There are no known related appeals and/or interferences.

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(3) Status of Claims

Claims 1-10 are pending. Claims 1-5, 9, and 10 are under consideration. Claims 6-8 have been withdrawn from consideration.

(4) Status of Amendments

Claims 1 and 5 were amended after final rejection in the Amendment filed on August 1, 2005. The Advisory Action mailed August 12, 2005 indicated that these claim amendments would be entered for purposes of appeal.

(5) Summary of Claimed Subject Matter

Independent claim 1 relates to a solid-state detector that includes a pixilated semiconductor detector, such as described in para. [0028]. The pixilated semiconductor detector has plurality of individual indium bumps arrayed on a surface of the detector, such as described in para. [0028]. The indium bumps are in electrical contact with the surface and are situated in defined locations on the surface, such as described in para. [0029]. The indium bumps can have a height of between 15 to 100μm, as described in para. [0012]

Independent claim 4 relates to a readout chip that includes a VLSI chip, such as described in paras. [0012] and [0018]. The

VLSI chip has a plurality of individual indium bumps arrayed on a surface of the chip, such as described in para. [0031]. The indium bumps are in electrical contact with the surface and are situated in defined locations on the surface, such as described in para. [0031]. The indium bumps have a height ranging from 15 to 100μm, as described in para. [0012].

Independent claim 5 relates to a hybrid detector comprising a pixilated detector in electrical contact with a VLSI chip, such as described in para. [0019]. The detector and the VLSI chip each have a surface with regions adapted to forming electrical contacts, such as described in para. [0019]. Electrical contacts formed from indium metal are made between the pixels of the semiconductor detector and regions on the VLSI chip corresponding thereto, such as described in para. [0019]. The surfaces of the pixilated detector and the VLSI chip are separated by 15 to 100μm, such as described in para. [0019] and in claim 5 as originally filed.

(6) Grounds of Rejection

In the final rejection mailed May 31, 2005, independent claims 1, 4, and 5 were rejected under 35 U.S.C. § 102 as anticipated by U.S. Patent No. 5,092,036 to Hu et al. (hereinafter "Hu"). Independent claims 1, 4, and 5 were also

rejected under 35 U.S.C. § 103(a) as obvious over Hu. The questions on appeal are

-whether claims 1, 4, and 5 are properly rejected as being anticipated by Hu; and

-whether claims 1, 4, and 5 are properly rejected as being obvious over Hu.

For purposes of this appeal, claims 1 and 4 stand or fall together as relating to devices that include indium bumps having a height ranging from 15 to 100μm. Claim 5 stands or falls independently as relating to a hybrid detector in which surfaces of a pixilated detector and a VLSI chip are separated by 15 to 100μm.

(7) Argument

Hu's Technology

Hu describes IR detectors made by sandwiching an interconnect pad 30 between a readout chip 44 and a detector chip 42. *See* Hu, col. 5, line 37-50.

Interconnect pad 30 houses an array of indium columns 40 that have been formed in metal tubes that traverse a high performance polymer film. *See Hu*, FIG. 2. The metal tubes are completely filled with molten indium by capillary action. *See Hu*, col. 5, line 33-36. The metal tubes protrude 20 μm from

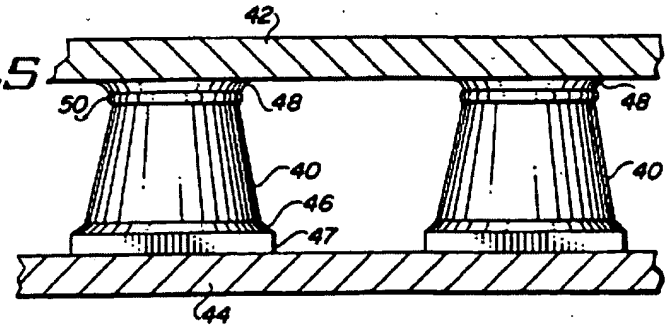
each side of the polymer film. *See Hu*, col. 2, line 23-25. The polymer film is itself 75 μm thick. *See Hu*, col. 2, line 21-22.

Indium columns 40 are therefore at least 115 μm (i.e., 20 μm + 75 μm + 20 μm) in height in interconnect pad 30.

To connect indium columns 40 to readout chip 44 and a detector chip 42, a first array of indium bumps 46 is deposited on an array of contact pads 47 on readout chip 44 and a second array of indium bumps 50 is formed on an array of contact mesas 48 on detector chip 42. *See Hu*, col. 5, line 37-40 and 46-50. Hu is silent as to the height of the arrays of indium bumps 46, 50, pads 47, and mesas 48. In another context, Hu does indicate that indium bumps have a typical height of 6-9 μm but not more than 10 μm. *See Hu*, col. 1, line 37-42.

Indium columns 40 are then cold welded to the first array of indium bumps 46 while still contained in the metal tubes of interconnect pad 30. *See Hu*, col. 5, line 40-46. After the metal tubes and the remainder of interconnect pad 30 are removed, indium columns 40 are subsequently cold-welded to the

FIG. 5



second array of indium bumps 50 to join chips 42, 44. *See Hu*, col. 5, 46-50. The resulting structure is illustrated in FIG. 5 of Hu, which is reproduced above.

Other than the express description of indium columns 40 being at least 115 μm in height before cold-welding, Hu is silent as to the net height of the combined indium structures formed by indium bumps 46, indium columns 40, and indium bumps 50. Hu is likewise silent as to the net separation distance between the surfaces of chips 42, 44, which are spaced apart by indium bumps 46, indium columns 40, indium bumps 50, pads 47, and mesas 48.

The Anticipation Rejections

"Anticipation under § 102 can be found only when the reference discloses exactly what is claimed..." *See Titanium Metals Corp. v. Banner*, 778 F.2d 775 (Fed. Cir. 1985). *See also* MPEP § 2131.

Hu simply does not disclose the claimed subject matter. He is silent as to the net height of the combined indium structures and as to the net separation distance between chips 42, 44. Rather, Hu only identifies the initial height of one component of the combined indium structures, namely, indium columns 40. This initial height of indium columns 40 is larger than the

claimed heights. Any contention that Hu does disclose the claimed subject matter is pure speculation and insufficient to support an anticipation rejection.

An example of such speculation is found in the Advisory Action mailed August 12, 2005, which contends that the indium columns in Hu's detector compress, presumably during cold-welding when pressure is applied, to arrive at the claimed range. However, Hu does not describe that any inelastic - and hence irreversible - compression of his indium columns occurs during the cold-welding process. Indeed, during the first cold-welding to indium readout chip bumps 46, Hu's indium columns are contained in the supporting metal tubes of interconnect pad 30. Further, no compression or other deformation of Hu's indium columns is illustrated in FIGS. 5, 7, or 8. The speculation that indium columns 40 compress is thus pure conjecture and not supported by Hu's disclosure.

Further, even if some compression of Hu's 115 μm tall indium columns were to occur (which Applicant does not concede), the rejection neglects that the final height of Hu's combined indium structures is the sum of the heights of indium bumps 46, indium columns 40, and indium bumps 48. There is simply no basis to believe that this combined height is between 15 to 100 μm, especially given that one component (i.e., indium columns

40) has an initial height of 115 μm, well in excess of the claimed range.

Further, in regard to claim 5, even if the height of the combined indium structure were not sufficient to ensure that the respective surfaces of chips 42, 44 were spaced apart by more than 100 μm, chips 42, 44 include additional features that further increase their spacing. In particular, pads 47 and mesas 48 also space the surfaces of chips 42, 44 apart, as clearly shown in Hu's FIG. 5.

On these bases, it is apparent that Hu does not disclose a pixilated semiconductor detector or a VLSI chip which include indium bumps that have a height of between 15 to 100 μm. Accordingly, the anticipation rejections of claims 1 and 4 are improper and must be withdrawn. It is also apparent Hu does not disclose that the surfaces of Hu's chips 42, 44 are separated by 15 to 100μm. Accordingly, the anticipation rejections of claim 5 is improper and must be withdrawn.

The Obviousness Rejections

The PTO has the burden of establishing a *prima facie* case of obviousness. *See In re Mayne*, 104 F.3d 1339, 1341 (Fed. Cir. 1997). A *prima facie* case of obviousness arises when the ranges of a claimed composition overlap the ranges disclosed in the

prior art or when the differences therebetween are so minor that one skilled in the art would have expected them to have the same properties. *See In re Peterson*, 315 F.3d 1325, 1329 (Fed. Cir. 2003); *In re Geisler*, 116 F.3d 1465, 1469 (Fed. Cir. 1997); *Titanium Metals Corp. v. Banner*, 778 F.2d at 783.

As discussed above, there is no reason to believe that Hu's disclosure overlaps with the claimed range. Hu is silent as to the final dimensions of his composite structure. Further, Hu's indium columns 40 are initially outside the claimed range. The indium columns are then cold welded to two different indium bumps. Hu does not describe that cold-welding results in inelastic deformation of the indium columns. Also, the final height of the indium structure is the sum of the heights of the indium columns and the two indium bumps. This composite structure would appear likely to be larger than the initial size of the indium column alone and hence further removed from the claimed range. This is especially true for claim 5, since pads 47 and mesas 48 space the surfaces of chips 42, 44 yet further apart and further away from the claimed range. On these bases, the PTO has failed to carry the burden of establishing a *prima facie* case of obviousness on the basis of an overlap with the claimed range.

The PTO has also failed to carry the burden of establishing that differences between Hu's disclosure and the claimed range are minor, or that one skilled in the art would have expected them to have the same properties. In the absence of information regarding Hu's composite structure, there is no basis to believe that the differences are minor. Any assertions regarding the dimensions of Hu's composite structure are pure conjecture. Instead, given the express teaching that a component of the composite structure is outside the claimed range and then added, in series, to additional components, it appears that Hu's composite structure is well removed from the claimed range.

Moreover, Hu himself describes that the height of the connectors between chips is an important design feature. In particular, Hu describes that indium connectors should be "made taller or longer." The increased height could result in a "more compliant arrangement" that "is expected to exhibit more tolerance for the effects of thermal expansion and contraction during repeated temperature excursions between room temperature and operating temperature." *See Hu*, col. 1, line 58-68.

Applicant's own specification also points out that the height of connectors between chips is an important design feature. In particular, Applicant describes that electronic noise is a significant limiting factor in ability of CZT

detectors to image radiation. Higher bump heights may lower the capacitance and the lower electronic noise in such detectors. *See* para. [0017].

Thus, the both Hu and Applicant's own disclosure describe that the height of the connectors between chips is an important design feature. Given that these references describe that both compliance and capacitance depend on distance, Applicant submits that one skilled in the art would have expected Hu's connectors to have different compliances and capacitances than those within the claimed ranges.

Since the PTO has failed to carry its burden of establishing that the claimed ranges overlap with Hu's composite structure, or that the differences between the claimed ranges and Hu's composite structure are so minor that one skilled in the art would have expected them to have the same properties, Applicant submits that a *prima facie* case of obviousness has not been established.

Even if the claimed ranges were *prima facie* obvious over Hu, an applicant may rebut by showing that the prior art teaches away from the claimed invention in any material respect. *See In re Geisler*, 116 F.3d 1465, 1469 (Fed. Cir. 1997) (quoting *In re Malagari*, 499 F.2d 1297, 1303 (CCPA 1974)).

Hu is clearly directed at increasing the compliance of the connections between his chips. *See, e.g., Hu*, col. 1, line 58-68 (describing that a "more compliant arrangement is expected to exhibit more tolerance for the effects of thermal expansion and contraction during repeated temperature excursions"); *Hu*, col. 2, line 64 - col. 3, line 5 (describing that "ultra-tall indium" provide a "compliant structural coupling" and avoid "the deleterious results of thermal fatigue as described above--breaking off pieces of contacts, pulling contact pads away from the substrate, warpage, etc.")

Hu also clearly describes that increased compliance is to be achieved with increased height. *See, e.g., Hu*, col. 3, line 34-46 (describing that multiple indium columns can be connected end-on-end to form yet taller indium columns, thereby "providing additional spacing between the detector and readout chips with correspondingly increased compliance to accommodate the thermal expansion and contraction.").

Rather than providing the increased height and increased compliance espoused by Hu, the claimed ranges appear to be smaller than the smallest disclosed implementation described in Hu. Accordingly, upon reviewing Hu, one of ordinary skill would be led away from the claimed ranges. In particular, the claimed range would be expected to have a lower compliance and increased

"deleterious results of thermal fatigue." Thus, even if a *prima facie* case of obviousness were established (which applicant does not concede), it is rebutted by the teachings in Hu away from the claimed subject matter.

Accordingly, the obviousness rejections of claims 1, 4, and 5 are improper and must be withdrawn.

Other Issues

During the course of prosecution, rejections have been based on two contentions that are tangential to the patentability analysis discussed above. For the sake of completeness, Applicant now addresses these contentions.

A first such contention is that indium bumps that are larger than 100 μm are more desirable than indium bumps that are smaller that 100 μm. On the basis of this alleged superiority of larger indium bumps, bumps that are smaller that 100 μm are allegedly not patentable.

Even if it is true that larger indium bumps are more desirable than smaller indium bumps in every application (which applicant does not concede), this contention neglects the standard of non-obviousness that has been applied since *Graham* in 1966. In particular, "subjective feelings" regarding the desirability of an invention are largely irrelevant as to

whether inventions are patentable. Rather, patentability is to be determined primarily based on the scope and content of the prior art and on the level of skill in the art. *Graham et al. v. John Deere Co. of Kansas City et al.*, 383 U.S. 1 (1966).

As discussed above, the scope and content of Hu neither describes nor suggests the claimed invention. The proposed reliance on mere "subjective feelings" or "obvious to try" is insufficient to establish obviousness and maintain the rejections.

The second such contention asserts that since para. [0013] of the specification describes "arrayed features having a height of about 10 to about 200μm," the claims must also encompass such features.

Applicant submits that the plain language of the claims clearly excludes indium bumps having a height of 200 microns. Additional implementations in the specification expressly outside of the scope of the claims cannot be used as a basis to reject the claims.

The brief fee of $250 is enclosed. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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Appendix of Claims

1. A solid-state detector comprising:

a pixilated semiconductor detector having plurality of individual indium bumps arrayed on a surface of the detector, wherein the indium bumps are in electrical contact with the surface and are situated in defined locations on the surface, and the indium bumps have a height of between 15 to 100μm.

2. The solid-state detector of claim 1 wherein the indium bumps have a height of between 20 to about 70μm.

3. The solid-state detector of claim 1 wherein the pixilated detector is selected from the group consisting of Si, Ge, HgI, CdTe, and CdZnTe semiconductors.

4. A readout chip comprising a VLSI chip having a plurality of individual indium bumps arrayed on a surface of the chip, wherein the indium bumps are in electrical contact with the surface and are situated in defined locations on the surface, and the indium bumps have a height ranging from 15 to 100μm.

5. A hybrid detector comprising a pixilated detector in electrical contact with a VLSI chip, wherein the detector and the VLSI chip each have a surface with regions adapted to

forming electrical contacts, and wherein electrical contacts formed from indium metal are made between the pixels of the semiconductor detector and regions on the VLSI chip corresponding thereto, and wherein the surfaces of the pixilated detector and the VLSI chip are separated by 15 to 100μm.

Claims 6 - 8. Withdrawn

9. The solid-state detector of claim 1 wherein the indium bumps have been formed by evaporating indium metal under vacuum through holes in a mask onto the detector.

10. The solid-state detector of claim 1 wherein the indium bumps are between 50 and 55 μm in diameter.